CLAIMS:

1. A method of forming a capacitor on a semiconductor substrate, the method including the steps of:

(a) forming a device body in the semiconductor substrate using a first type of dopant material;

(b) forming a dielectric layer over the device body;

(c) forming an electrode layer over the dielectric layer in an area defined by an upper surface of the device body;

(d) forming a first lateral region in the semiconductor substrate along a first lateral side of the device body, the first lateral region being in electrical contact with the device body along the first lateral side of the device body and containing the first type of dopant material at a level relatively higher than is characteristic of the device body;

(e) forming a second lateral region in the semiconductor substrate along a second lateral side of the device body opposite the first lateral side, the second lateral region being in electrical contact with the device body along the second lateral side of the device body and containing the first type of dopant material at a level relatively higher than is characteristic of the device body;

(f) forming an insulating layer over the electrode layer, first lateral region, and second lateral region;

(g) electrically connecting the first and second lateral regions to a first supply voltage potential at a first longitudinal end of the device body; and

(h) electrically connecting the electrode layer to a second supply voltage potential at a second longitudinal end of the device body opposite to the first longitudinal end of the device body.

2. The method of Claim 1 wherein the first type of dopant material comprises N-type material and the step of forming the device body includes implanting the N-type material in a bulk P-type semiconductor substrate.

3. The method of Claim 2 further including:

(a) forming an N-well in the semiconductor substrate prior to forming the device body; and

(b) wherein the step of forming the device body includes performing an additional N-type material implantation in a selected area of the N-well.

4. The method of Claim 1 further including the step of forming a first end region in the semiconductor substrate abutting the first longitudinal end of the device body and contacting the first and second lateral regions adjacent to the first longitudinal end of the device body, the first end region being formed using the first type of dopant material.

5. The method of Claim 4 wherein the step of electrically connecting the first lateral region and the second lateral region to the first supply voltage potential comprises forming ground potential contacts to the first end region.

6. The method of Claim 1 further including the steps of forming a buried oxide layer in the semiconductor substrate and forming side oxide regions in the semiconductor substrate in areas bounding an area for the capacitor, the steps of forming the buried oxide layer and side oxide regions being performed prior to forming the device body.

7. The method of Claim 6 wherein the first type of dopant material comprises N-type material and the step of forming the device body includes implanting the N-type material in the volume of the semiconductor substrate defined between the side oxide regions.

8. The method of Claim 7 wherein the step of forming the first and second lateral regions comprises implanting additional N-type material in areas defined between lateral sides of the device body and the side oxide regions.

9. The method of Claim 7 wherein the step of forming the device body includes an additional N-type material implantation in the volume of the semiconductor substrate defined between the side oxide regions.

10. The method of Claim 7 further including the step of forming a first end region in the semiconductor substrate abutting the first longitudinal end of the device body and contacting the first and second lateral regions adjacent to the first longitudinal end of the device body, the first end region being formed using N-type material.

11. The method of Claim 10 wherein the step of electrically connecting the first lateral region and the second lateral region to the first supply voltage potential comprises forming ground potential contacts to the first end region.

12. A method of forming a capacitor on a semiconductor substrate together with an integrated circuit comprising a plurality of circuit devices, the method including the steps of:

(a) concurrently forming a capacitor device body and a plurality of additional device bodies in the semiconductor substrate using a first type of dopant material, each additional device body corresponding to a respective one of the circuit devices;

(b) concurrently forming a dielectric layer over the capacitor device body and over each additional device body;

(c) concurrently forming an electrode layer over the dielectric layer in an area defined by an upper surface of the capacitor device body and in each respective area defined by an upper surface of each respective additional device body;

(d) forming a first lateral region and a second lateral region in the semiconductor substrate along opposite lateral sides of the capacitor device body and concurrently forming a respective drain region and a respective source region in the semiconductor substrate along opposite sides of each respective additional device body, the first lateral region, second lateral region, each respective drain region, and each respective source region being formed using the first type of dopant material at a level relatively higher than is characteristic of the capacitor device body and each respective additional device body;

(e) forming an insulating layer over the electrode layer, first lateral region, second lateral region, each respective drain region, and each respective source region;

(f) electrically connecting the first and second lateral regions to a first supply voltage potential at a first longitudinal end of the capacitor device body; and

(g) electrically connecting the electrode layer situated over the upper surface of the capacitor device body to a second supply voltage potential at a second longitudinal end of the capacitor device body opposite to the first longitudinal end of the capacitor device body.

13. The method of Claim 12 wherein the first type of dopant material comprises N-type material and the step of concurrently forming the capacitor device body and each respective additional device body includes implanting the N-type material in a bulk P-type semiconductor substrate.

14. The method of Claim 12 wherein the step of forming the first lateral region, second lateral region, each drain region, and each source region also includes concurrently forming a first end region in the semiconductor substrate abutting the first longitudinal end of the capacitor device body and contacting the first and second lateral regions adjacent to the first longitudinal end of the capacitor device body.

15. The method of Claim 12 further including the steps of:

(a) forming a buried oxide layer in the semiconductor substrate, the buried oxide layer being formed in an area for the capacitor and in a respective area for each respective circuit device;

(b) forming a first set of side oxide regions in the semiconductor substrate for the capacitor, the first set of side oxide regions bounding the area for the capacitor;

(c) forming a respective additional set of side oxide regions in the semiconductor substrate for each respective circuit device, the respective additional set of side oxide regions bounding the area for the respective circuit device; and

(d) wherein the steps of forming the buried oxide layer and each set of side oxide regions are performed prior to forming the capacitor device body and each additional device body.

16. The method of Claim 15 wherein the first type of dopant material comprises N-type material and the step of forming the capacitor device body and each additional device body includes implanting the N-type material in the areas of the semiconductor substrate defined within each respective set of side oxide regions.

17. The method of Claim 16 wherein the step of forming the first lateral region and second lateral region comprises implanting additional N-type material in areas defined between lateral sides of the capacitor device body and the first set of side oxide regions, and wherein the step of forming each drain region and each source region comprises implanting additional N-type material in

areas defined between lateral sides of the respective additional device body and the respective additional set of side oxide regions.

18. A method for improving the frequency response of a decoupling capacitor in an integrated circuit, the decoupling capacitor including a device body analogous to the device body of a transistor included in the integrated circuit and being formed using a first type impurity material, the decoupling capacitor further including first and second lateral regions analogous to the source and drain regions of the transistor included in the integrated circuit chip, the method comprising the step of:

(a) adding additional first type impurity material to an area in the substrate for the decoupling capacitor device body, the additional first type impurity material resulting in a region on the substrate for the decoupling capacitor device body that is more highly doped than a region on the substrate for the transistor device body.

19. The method of Claim 18 wherein the decoupling capacitor device body is formed in an N-well formed on a P-type substrate.

20. The method of Claim 18 wherein the decoupling capacitor device body comprises a region of N-type material formed above a buried oxide layer of a silicon-on-insulator integrated circuit.